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A EELS nanoanalytical investigation of high-*k* dielectric gate stacks for the realization of III-V based MOSFET devices

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Friday 2 October, 2009
11.00am – 12 noon
Science Lecture Theatre S10, Building 25

Abstract

Electron energy loss spectroscopy (EELS) is the analysis of the energy distribution of electrons that have passed through the specimen and interact inelastically with it. It is a powerful technique that provides information on elemental composition and electronic structure in a particular area of the material. By combining EELS with scanning transmission electron microscopy (STEM) it is possible to get an elemental map of a particular area in the material. This gives a spectrum image (SI) where an EELS spectrum is collected at each point in the scan. SI imaging gives very detailed information on the local chemistry and composition with spatial resolution potentially at the atomic level.

Here this approach is applied to study the chemistry across Ga_2O_3/GdGaO oxide layers as grown and as processed. Such oxides form the dielectric gate stack currently used for the realization of III-V based electronic devices such as MOSFETs. A thin template layer of Ga_2O_3 unpins the Fermi Level and a thicker layer of GdGaO provides low leakage current.

Electrical properties in MOSFET devices are sensitive to the elemental distribution at the nanoscale in the dielectric gate stack and the interfaces across the channel and the oxide region. Hence a good understanding of the local composition and chemistry is required in order to make successful devices and optimise their performance.

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